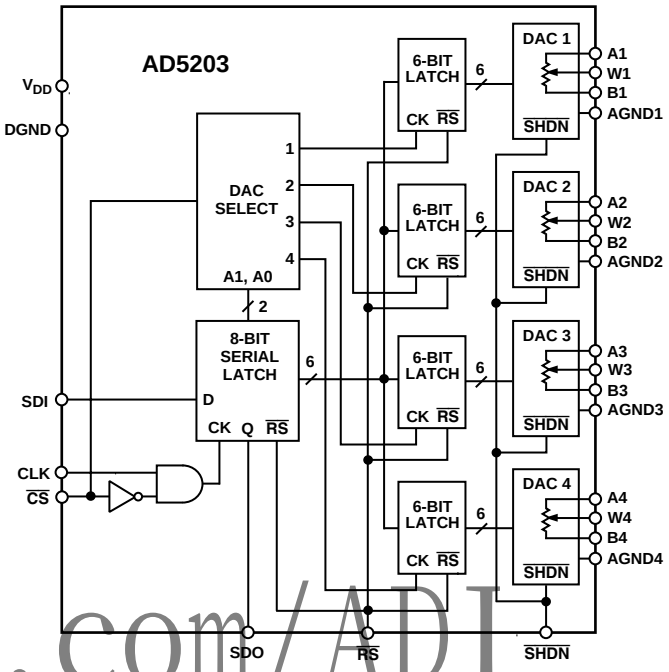
4-Channel, 64-Position Digital Potentiometer

AD5203

FEATURES
64 Position
Replaces Four Potentiometers
10 kΩ, 100 kΩ
Power Shutdown—Less than 5 μA
3-Wire SPI-Compatible Serial Data Input
10 MHz Update Data Loading Rate
+2.7 V to +5.5 V Single Supply Operation
Midscale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Programmable Filters, Delays, Time Constants
Volume Control, Panning
Line Impedance Matching
Power Supply Adjustment

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD5203 provides a quad channel, 64-position digitally-controlled variable resistor (VR) device. These parts perform the same electronic adjustment function as a potentiometer or variable resistor. The AD5203 contains four independent variable resistors in a 24-lead SOIC and the compact TSSOP-24 packages. Each part contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the controlling serial input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. Each variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A-to-B terminal resistance of 10 kΩ, or 100 kΩ has a ±1% channel-to-channel matching tolerance with a nominal temperature coefficient of 700 ppm/°C.

Each VR has its own VR latch which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial-input digital interface. Eight data bits make up the data word clocked into the serial input register. The data word is decoded where the first two bits determine the address of the VR latch to be loaded, the last 6-bits are data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple VR applications without additional external decoding logic.

The reset $\overline{RS}$ pin forces the wiper to the midscale position by loading 20_H into the VR latch. The $\overline{SHDN}$ pin forces the resistor to an end-to-end open circuit condition on terminal A and shorts the wiper to terminal B, achieving a microwatt power shutdown state. When shutdown is returned to logic-high the previous latch settings put the wiper in the same resistance setting prior to shutdown.

The AD5203 is available in a narrow body P-DIP-24, the 24-lead surface mount package, and the compact 1.1 mm thin TSSOP-24 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

For pin compatible higher resolution applications, see the 256-position AD8403 product.

REV. 0

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AD5203–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +3 V ± 10% or +5 V ± 10%, V_A = +V_{DD}, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications Apply to All VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = No Connect	–0.25	±0.1	+0.25	LSB
Resistor Nonlinearity Error[2]	R-INL	R_{WB}, V_A = No Connect	–0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		–30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		700		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R_{AB}		45	100	Ω
Nominal Resistance Match	$\Delta R/R_O$	CH 1 to CH 2, V_{AB} = V_{DD} , T_A = +25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications Apply to All VRs						
Resolution	N		6			Bits
Differential Nonlinearity Error[4]	DNL		–0.25	±0.1	+0.25	LSB
Integral Nonlinearity Error[4]	INL		–0.75	±0.1	+0.75	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 20_H		20		ppm/°C
Full-Scale Error	V_{WFSE}	Code = $3F_H$	–0.75	–0.2	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+0.1	+0.75	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		0		V_{DD}	V
Capacitance[6] Ax, Bx	C_A, C_B	f = 1 MHz, Measured to GND, Code = 20_H		75		pF
Capacitance[6] Wx	C_W	f = 1 MHz, Measured to GND, Code = 20_H		120		pF
Shutdown Supply Current[7]	I_{A_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = +5 V		45	100	Ω
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Output Logic High	V_{OH}	R_L = 2.2 kΩ to V_{DD}	V_{DD}–0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = +5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V, V_{DD} = +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or V_{IL} = 0.8 V, V_{DD} = +5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%		0.0002	0.001	%/%
	PSS	ΔV_{DD} = +3 V ± 10%		0.006	0.03	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW_10K	R_{AB} = 10 kΩ		600		kHz
	BW_100K	R_{AB} = 100 kΩ		71		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.003		%
V_W Settling Time	t_S_10K	V_A = V_{DD}, V_B = 0 V, ±1 LSB Error Band		2		µs
	t_S_100K	V_A = V_{DD}, V_B = 0 V, ±1 LSB Error Band		18		µs
Resistor Noise Voltage	e_{NWB}	R_{WB} = 5 kΩ, f = 1 kHz, $\overline{RS}$ = 0		9		nV/√Hz
		R_{WB} = 50 kΩ, f = 1 kHz, $\overline{RS}$ = 0		29		nV/√Hz
Crosstalk[11]	C_T	V_A = V_{DD}, V_B = 0 V		–65		dB
INTERFACE TIMING CHARACTERISTICS Applies to All Parts[6, 12]						
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock Level High or Low	10			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
CLK to SDO Propagation Delay[13]	t_{PD}	R_L = 2.2 kΩ, C_L < 20 pF	1		25	ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		10			ns
Reset Pulsewidth	t_{RS}		50			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

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NOTES
[1]Typicals represent average readings at +25°C and V_{DD} = +5 V.
[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 27 test circuit. $I_W = V_{DD}/R$ for both V_{DD} = +3 V or V_{DD} = +5 V.
[3]$V_{AB} = V_{DD}$, Wiper (V_W) = No connect.
[4]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See Figure 26 test circuit.
[5]Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6]Guaranteed by design and not subject to production test.
[7]Measured at the AX terminals. All AX terminals are open-circuited in shutdown mode.
[8]Worst case supply current consumed when all logic-input levels set at 2.4 V, standard characteristic of CMOS logic. See Figure 19 for a plot of I_{DD} vs. logic voltage inputs result in minimum power dissipation.
[9]P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[10]All dynamic characteristics use V_{DD} = +5 V.
[11]Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.
[12]See timing diagrams for location of measured values. All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using both V_{DD} = +3 V or +5 V. Input logic should have a 1 V/µs minimum slew rate.
[13]Propagation delay depends on value of V_{DD}, R_L and C_L. See Operation section.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V, +8 V
V_A, V_B, V_W to GND . . . . . 0 V, V_{DD}
I_{AB}, I_{AW}, I_{BW} . . . . . ±20 mA
Digital Input and Output Voltage to GND . . . . . 0 V, +8 V
Operating Temperature Range . . . . . –40°C to +85°C
Maximum Junction Temperature (T_J MAX) . . . . . +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . (T_J max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}
P-DIP (N-24) . . . . . 63°C/W
SOIC (SOL-24) . . . . . 70°C/W
TSSOP-24 . . . . . 143°C/W

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table I. Serial-Data Word Format

ADDR		DATA					
B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	D5	D4	D3	D2	D1	D0
MSB	LSB	MSB					LSB
2^7	2^6	2^5					2^0

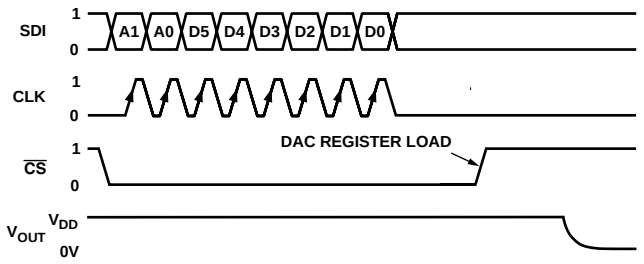

Figure 1a. Timing Diagram

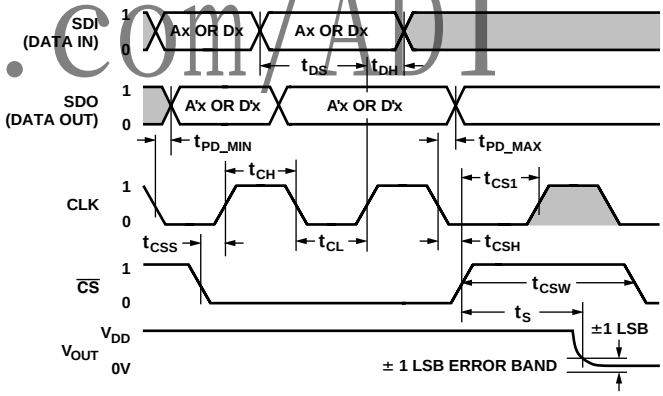

Figure 1b. Detail Timing Diagram

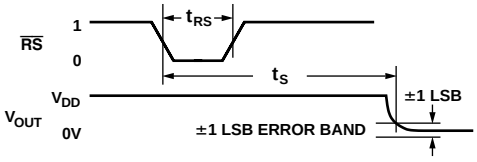

Figure 1c. Reset Timing Diagram

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5203 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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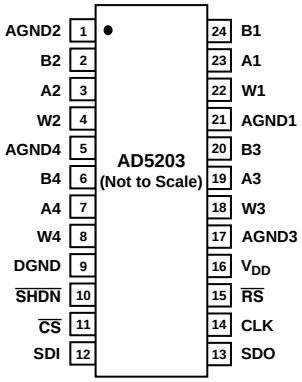
PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	AGND2	Analog Ground #2*
2	B2	B Terminal RDAC #2
3	A2	A Terminal RDAC #2
4	W2	Wiper RDAC #2, addr = 01_2
5	AGND4	Analog Ground #4*
6	B4	B Terminal RDAC #4
7	A4	A Terminal RDAC #4
8	W4	Wiper RDAC #4, addr = 11_2
9	DGND	Digital Ground*
10	$\overline{SHDN}$	Active Low Input. Terminal A open circuit. Shutdown controls Variable Resistors #1 through #4.
11	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high data in the serial input register is decoded based on the address bits and loaded into the target DAC register.
12	SDI	Serial Data Input
13	SDO	Serial Data Output. Open drain transistor requires pull-up resistor.
14	CLK	Serial Clock Input, positive edge triggered.
15	$\overline{RS}$	Active low reset to midscale; sets RDAC registers to 20_H.
16	V_{DD}	Positive power supply, specified for operation at both +3 V and +5 V.
17	AGND3	Analog Ground #3*
18	W3	Wiper RDAC #3, addr =10_2
19	A3	A Terminal RDAC #3
20	B3	B Terminal RDAC #3
21	AGND1	Analog Ground #1*
22	W1	Wiper RDAC #1, addr = 00_2
23	A1	A Terminal RDAC #1
24	B1	B Terminal RDAC #1

*All AGNDs must be connected to DGND voltage potential.

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ORDERING GUIDE

Model	kΩ	Temperature Range	Package Descriptions	Package Options
AD5203AN10	10	–40°C to +85°C	24-Lead Narrow Body Plastic DIP	N-24
AD5203AR10	10	–40°C to +85°C	24-Lead Wide Body (SOIC)	SOL-24
AD5203ARU10	10	–40°C to +85°C	24-Lead Thin Surface Mount Package (TSSOP)	RU-24
AD5203AN100	100	–40°C to +85°C	24-Lead Narrow Body Plastic DIP	N-24
AD5203AR100	100	–40°C to +85°C	24-Lead Wide Body (SOIC)	SOL-24
AD5203ARU100	100	–40°C to +85°C	24-Lead Thin Surface Mount Package (TSSOP)	RU-24

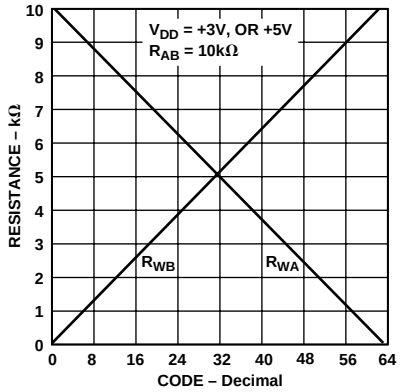

Figure 2. Wiper to End Terminal Resistance vs. Code

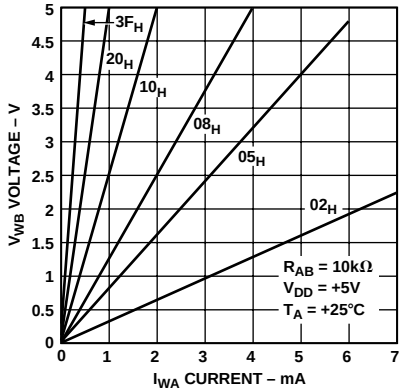

Figure 3. Resistance Linearity vs. Conduction Current

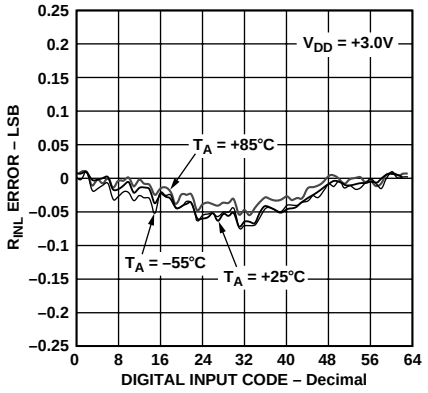

Figure 4. Resistance Step Position Nonlinearity Error vs. Code

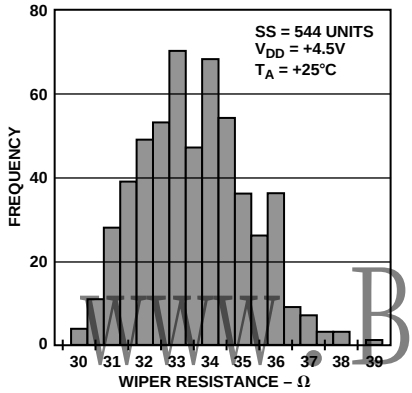

Figure 5. Wiper-Contact-Resistance Histogram

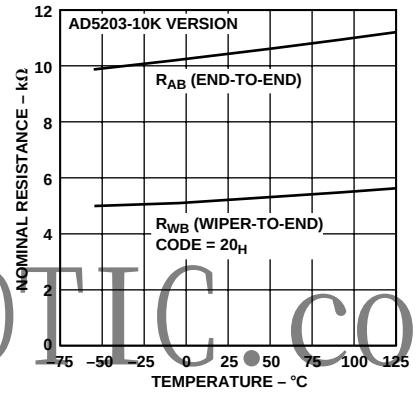

Figure 6. Nominal Resistance vs. Temperature

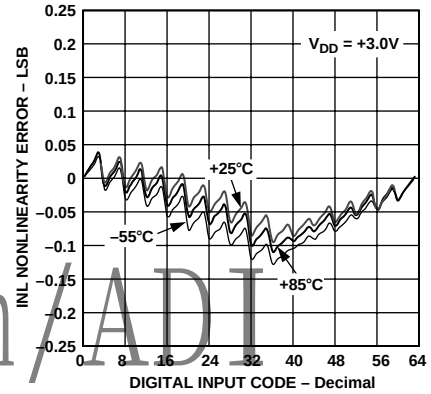

Figure 7. Potentiometer Divider Nonlinearity Error vs. Code

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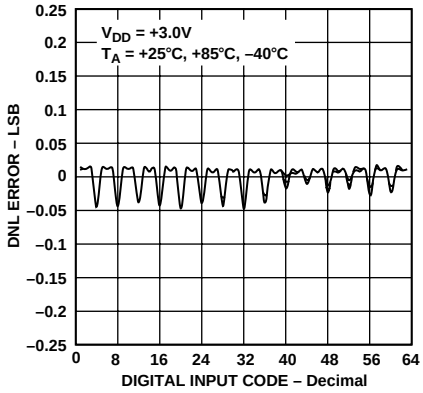

Figure 8. Potentiometer Divider Differential Nonlinearity Error vs. Code

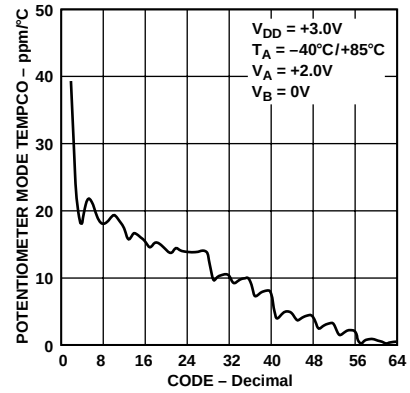

Figure 9. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco

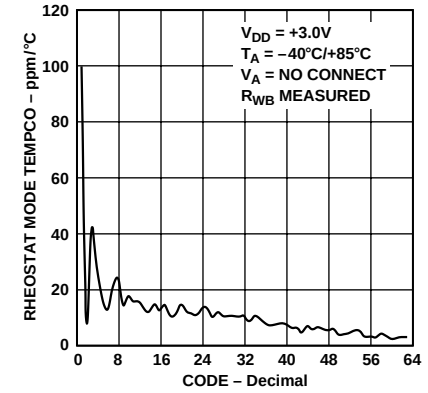

Figure 10. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco

AD5203–Typical Performance Characteristics

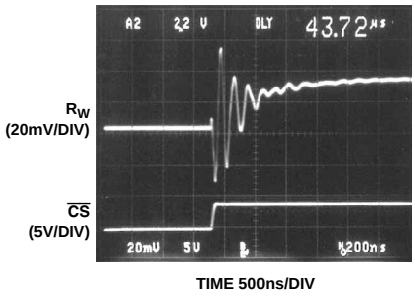

Figure 11. One Position Step Change at Half-Scale (Code 1F$_H$ to 20$_H$)

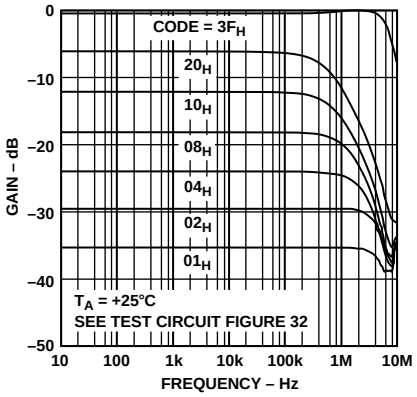

Figure 12. Gain vs. Frequency for R = 10 kΩ

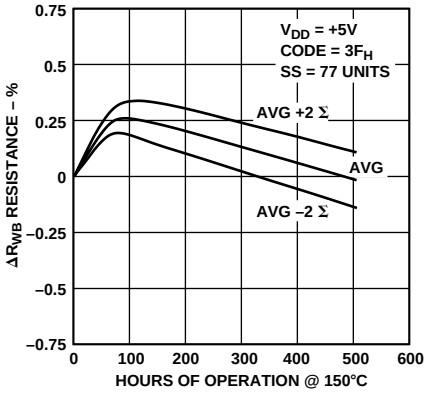

Figure 13. Long-Term Drift Accelerated by Burn-In

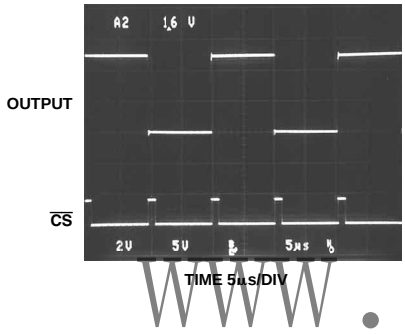

Figure 14. Large Signal Settling Time

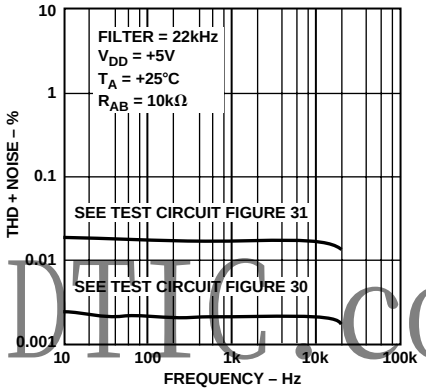

Figure 15. Total Harmonic Distortion Plus Noise vs. Frequency

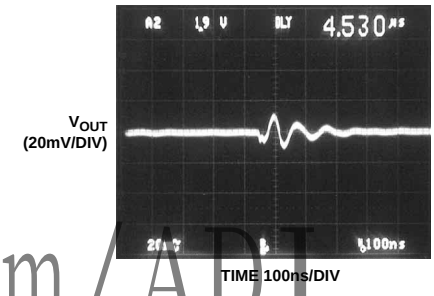

Figure 16. Digital Feedthrough vs. Time

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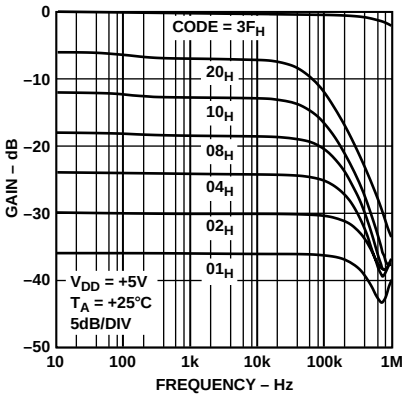

Figure 17. 100 kΩ Gain vs. Frequency vs. Code

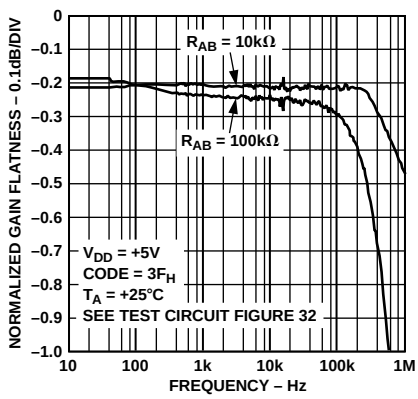

Figure 18. Normalized Gain Flatness vs. Frequency

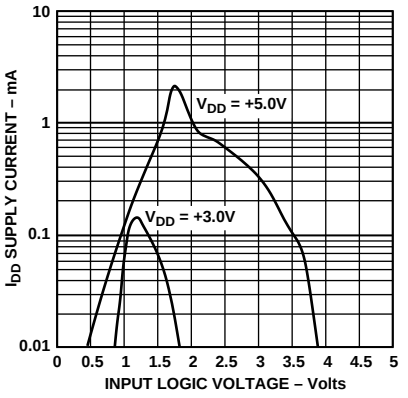

Figure 19. Supply Current vs. Logic Input Voltage

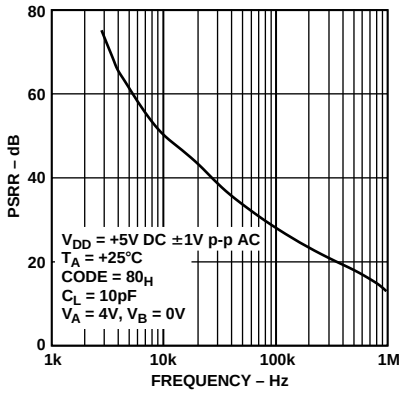

Figure 20. Power Supply Rejection vs. Frequency

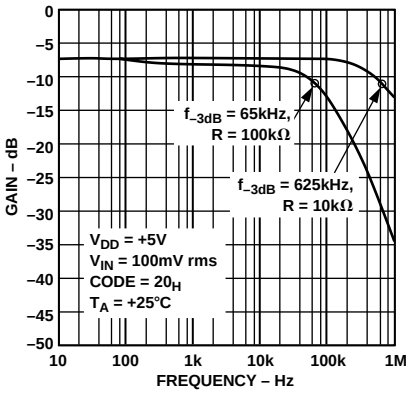

Figure 21. –3 dB Frequency at Half-Scale

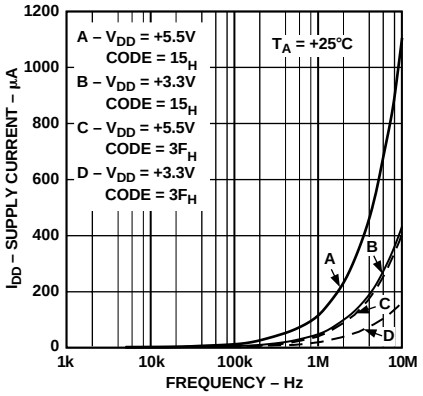

Figure 22. Supply Current vs. Clock Frequency

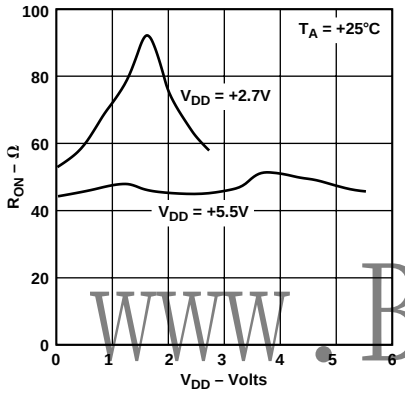

Figure 23. Incremental Wiper ON Resistance vs. V_{DD}

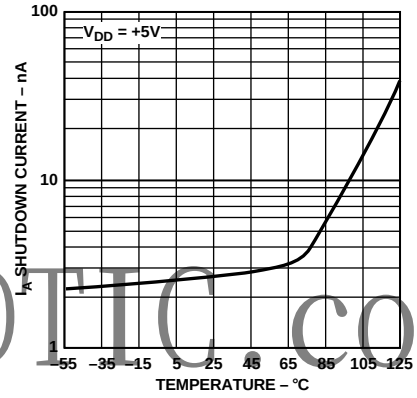

Figure 24. Shutdown Current vs. Temperature

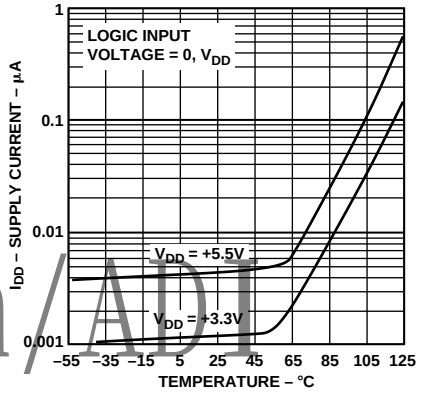

Figure 25. Supply Current vs. Temperature

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AD5203–Parametric Test Circuits

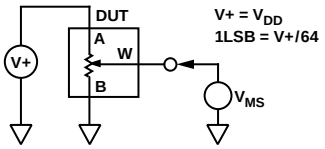

Figure 26. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

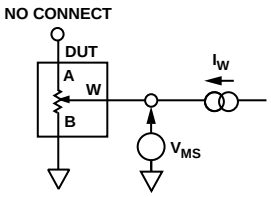

Figure 27. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

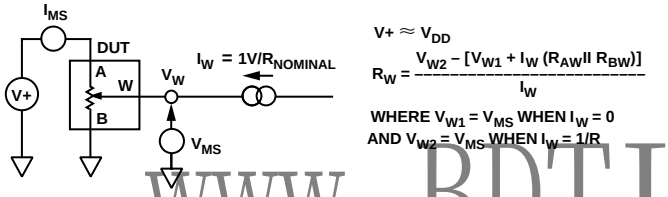

Figure 28. Wiper Resistance Test Circuit

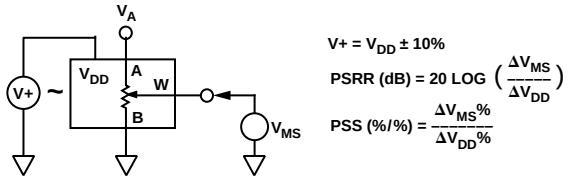

Figure 29. Power Supply Sensitivity Test Circuit (PSS, PSRR)

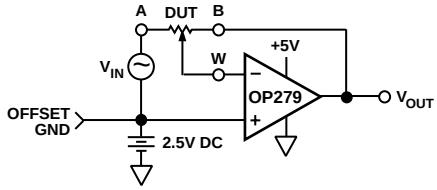

Figure 30. Inverting Programmable Gain Test Circuit

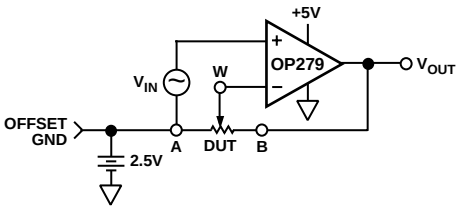

Figure 31. Noninverting Programmable Gain Test Circuit

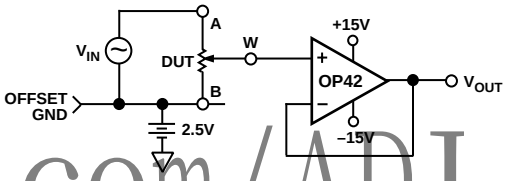

Figure 32. Gain vs. Frequency Test Circuit

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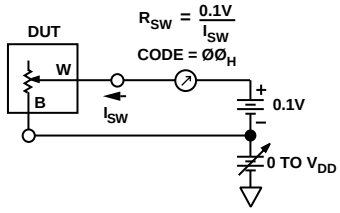

Figure 33. Incremental ON Resistance Test Circuit

OPERATION

The AD5203 provides a quad channel, 64-position digitally-controlled variable resistor (VR) device. Changing the programmed VR settings is accomplished by clocking in an 8-bit serial data word into the SDI (Serial Data Input) pin. The format of this data word is two address bits, MSB first, followed by six data bits, MSB first. Table I provides the serial register data word format. The AD5203 has the following address assignments for the ADDR decode, which determines the location of VR latch receiving the serial register data in Bits B5 through B0:

$$VR\# = A1 \times 2 + A0 + 1$$

VR outputs can be changed one at a time in random sequence. The serial clock running at 10 MHz makes it possible to load all four VRs in under 3.2 µs (8 × 4 × 100 ns) for the AD5203. The exact timing requirements are shown in Figure 1.

The AD5203 resets to a midscale by asserting the $\overline{RS}$ pin, simplifying initial conditions at power-up. Both parts have a power shutdown $\overline{SHDN}$ pin that places the RDAC in a zero power consumption state where terminals Ax are open-circuited and the wiper Wx is connected to Bx, resulting in only leakage currents being consumed in the VR structure. In shutdown mode the VR latch settings are maintained so that, returning to operational mode from power shutdown, the VR settings return to their previous resistance values.

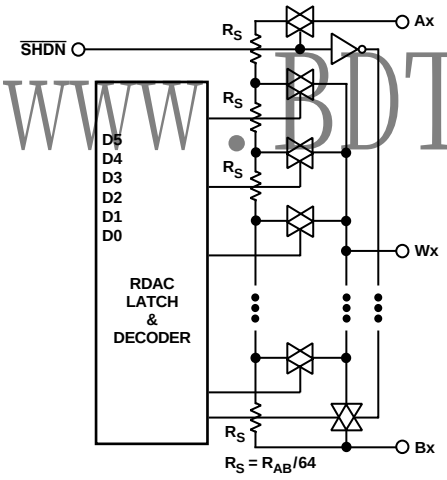

Figure 34. Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B are available with values of 10 kΩ, and 100 kΩ. The final digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 100 kΩ = 100. The nominal resistance (R_{AB}) of the VR has 64 contact points accessed by the wiper terminal, plus the B terminal contact. The 6-bit data word in the RDAC latch is decoded to select one of the 64 possible settings. The wiper's first connection starts at the B terminal for data 00_H. This B–terminal connection has a wiper contact resistance of 45 Ω. The second connection (10 kΩ part) is the first tap point located at 201 Ω [= R_{BA}(nominal resistance)/64 + R_W = 156 Ω + 45 Ω)] for data 01_H. The third connection is the next tap point representing 312 + 45 = 357 Ω for data 02_H. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 9889 Ω. The wiper does not directly connect to the B Terminal. See Figure 34 for a simplified diagram of the equivalent RDAC circuit.

The general transfer equation that determines the digitally programmed output resistance between Wx and Bx is:

$$R_{WB}(Dx) = (Dx)/64 \times R_{BA} + R_W \quad (1)$$

where Dx is the data contained in the 6-bit RDACx latch and R_{BA} is the nominal end-to-end resistance.

For example, when V_B = 0 V and A–terminal is open circuit the following output resistance values will be set for the following RDAC latch codes (applies to the 10K potentiometer):

D (DEC)	R_{WB} (Ω)	Output State
63	9889	Full-Scale
32	5045	Midscale ($\overline{RS}$ = 0 Condition)
1	201	1 LSB
0	45	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 45 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum value of 5 mA to avoid degradation or possible destruction of the internal switch contact.

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Like the mechanical potentiometer the RDAC replaces, it is totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used the B–terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(Dx) = (64\text{-}Dx)/64 \times R_{BA} + R_W \quad (2)$$

where *Dx* is the data contained in the 6-bit RDACx latch and R_{BA} is the nominal end-to-end resistance. For example, when V_A = 0 V and B–terminal is tied to the wiper W, the following output resistance values will be set for the following RDAC latch codes:

D (DEC)	R_{WA} (Ω)	Output State
63	201	Full-Scale
32	5045	Midscale ($\overline{RS}$ = 0 Condition)
1	9889	1 LSB
0	10045	Zero-Scale

The typical distribution of R_{BA} from channel to channel matches within ±1%. However, device-to-device matching is process-lot-dependent, having a ±30% variation. The change in R_{BA} with temperature has a 700 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example connecting A–terminal to +5 V and B–terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts up to 1 LSB less than +5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 64 position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(Dx) = Dx/64 \times V_{AB} + V_B$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors not the absolute value, therefore the drift improves to 20 ppm/°C.

DIGITAL INTERFACING

The AD5203 contains a standard three-wire serial input control interface. The three inputs are clock (CLK), $\overline{CS}$ and serial data input (SDI). The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means. The Figure 35 block diagram shows more detail of the internal digital circuitry. When $\overline{CS}$ is taken active low the clock loads data into the serial register on each positive clock edge, see Table III.

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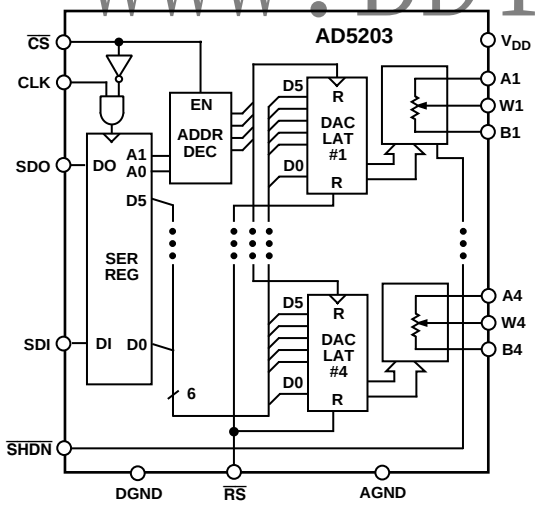

Figure 35. Block Diagram

The serial-data-output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. The pull-up resistor termination voltage may be larger than the V_{DD} supply of the AD5203 SDO output device, e.g., the AD5203 could operate at V_{DD} = 3.3 V and the pull-up for interface to the next device could be set at +5 V. This allows for daisy chaining several RDACs from a single processor serial data line. Clock period needs to be increased when using a pull-up resistor to the SDI pin of the following device in the series. Capacitive loading at the daisy chain node SDO-SDI between devices must be accounted for to successfully transfer data. When daisy chaining is used, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers insuring that the address bits and data bits are in the proper decoding location. This would require 16 bits of address and data complying to the word format provided in Table I if two AD5203 four-channel RDACs are daisy chained. During shutdown, $\overline{SHDN}$ the SDO output pin is forced to the off (logic high state) to disable power dissipation in the pull-up resistor. See Figure 37 for equivalent SDO output circuit schematic.

Table II. Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect, enables SDO pin.
P	L	H	H	Shift one bit in from the SDI pin. The eighth previously entered bit is shifted out of the SDO pin.
X	P	H	H	Load SR data into RDAC latch based on A1, A0 decode (Table III).
X	H	H	H	No Operation.
X	X	L	H	Sets all RDAC latches to midscale, wiper centered and SDO latch cleared.
X	H	P	H	Latches all RDAC latches to 20_H.
X	H	H	L	Open circuits all Resistor A–terminals, connects W to B, turns off SDO output transistor.

NOTE: P = positive edge, X = don't care, SR = shift register.

Table III. Address Decode Table

A1	A0	Latch Decoded
0	0	RDAC#1
0	1	RDAC#2
1	0	RDAC#3
1	1	RDAC#4

The data setup and data hold times in the specification table determine the data valid time requirements. The last eight bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. At the same time $\overline{CS}$ goes high it gates the address decoder which enables one of four positive edge triggered RDAC latches, see Figure 36 detail.

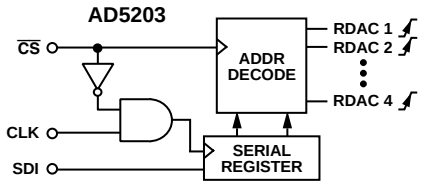

Figure 36. Equivalent Input Control Logic

The target RDAC latch is loaded with the last six bits of the serial data word completing one RDAC update. Four separate 8-bit data words must be clocked in to change all four VR settings.

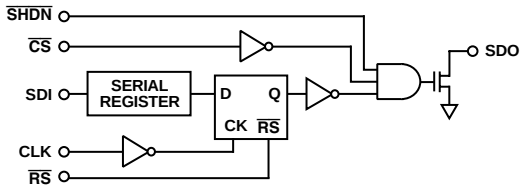

Figure 37. Detail, SDO Output Schematic of the AD5203

All digital inputs are protected with a series input resistor and parallel Zener ESD structure shown in Figure 38. Applies to digital input pins $\overline{CS}$, SDI, SDO, $\overline{RS}$, $\overline{SHDN}$, CLK.

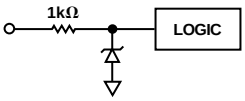

Figure 38. Equivalent ESD Protection Circuit

DYNAMIC CHARACTERISTICS

The total harmonic distortion plus noise (THD+N) measures 0.003% using an offset ground with a rail-to-rail OP279 inverting op amp test circuit, see Figure 30. Figure 15 plots THD versus frequency for both inverting and noninverting amplifier topologies. Thermal noise is primarily Johnson noise, typically 9 nV/$\sqrt{Hz}$ for the 10 kΩ version measured at 1 kHz. For the 100 kΩ device, thermal noise measures 29 nV/$\sqrt{Hz}$. Channel-to-channel crosstalk measures less than –65 dB at f = 100 kHz. To achieve this isolation, the extra ground pins (AGND) located between the potentiometer terminals (A, B, W) must be connected to circuit ground. The AGND and DGND pins should be at the same voltage potential. Any unused potentiometers in a package should be connected to ground. Power supply rejection is typically –50 dB at 10 kHz (care is needed to minimize power supply ripple injection in high accuracy applications).

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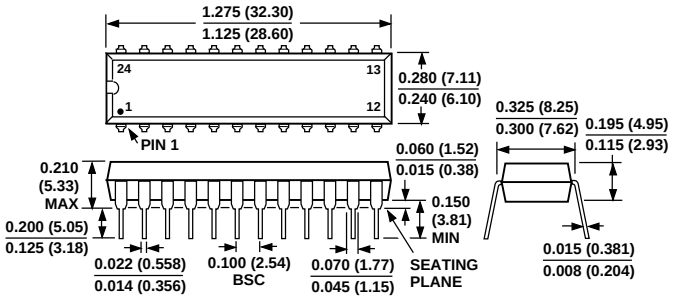
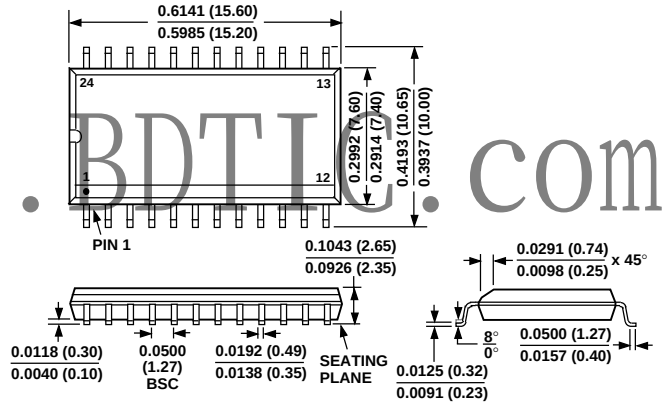
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Narrow Body Plastic DIP
(N-24)



24-Lead SOIC
(SOL-24)



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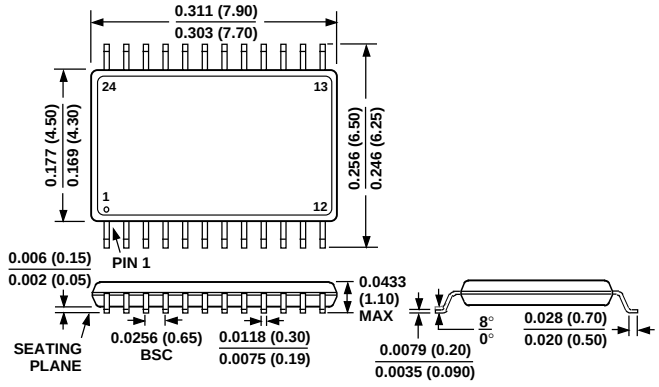
24-Lead Thin Surface Mount TSSOP
(RU-24)



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